

L1121 CompactFlash®/PC Card Interface Chip

OVERVIEW

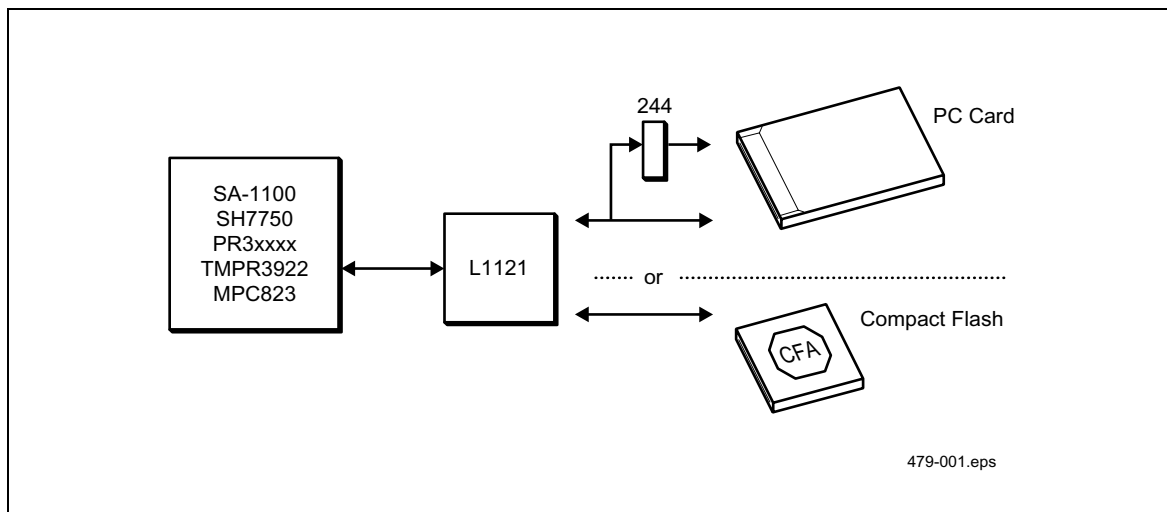
The L1121 provides a glueless interface between the LinkUp L7200, Intel SA-1100, Toshiba TMPR3922U, Hitachi SH7750, Motorola MPC823, and Philips PR3xxxx series integrated processors and one PC Card device. Because the CompactFlash interface is a subset of the PC Card interface, CompactFlash devices are also supported. The L1121 performs the 3V to 5V and 5V to 3V signal conversion and power switching with controlled slew rate. This results in a much smaller board space requirement and lower power. Optional use of an external power switch from Temic, TI, or Maxim is supported, for those applications which require higher socket voltage. The L1121 can also support PCMCIA 2.1 with two additional external buffers. One on-chip 8-bit DAC is provided for LCD contrast control.

- Glueless interface to popular system controllers for handheld and portable applications:
 - LinkUp L7200
 - Intel SA-1100
 - Philips PR3xxxx
 - Hitachi SH7750
 - Toshiba TMPR3922U
 - Motorola MPC823
- 3V to 5V and 5V to 3V signal conversion
- On-chip 3V and 5V switch for socket power
- Optional control of external switch for socket power
- Supports both 3V and 5V cards
- Low-power 8-bit D/A converter
- Edge- or level-sensitive interrupts
- Ultra low-power CMOS design
- 144-pin TQFP or FBGA package

FEATURES

- CompactFlash/PC Card interface
 - Allows hot insertion
 - Reduces power dissipation
 - Reduces board real estate

Figure 1. Example System Configurations Using the L1121 Interface Chip



TYPICAL APPLICATIONS

Figure 2. Interface to L7200 Using Off-chip Power Switches for One Slot

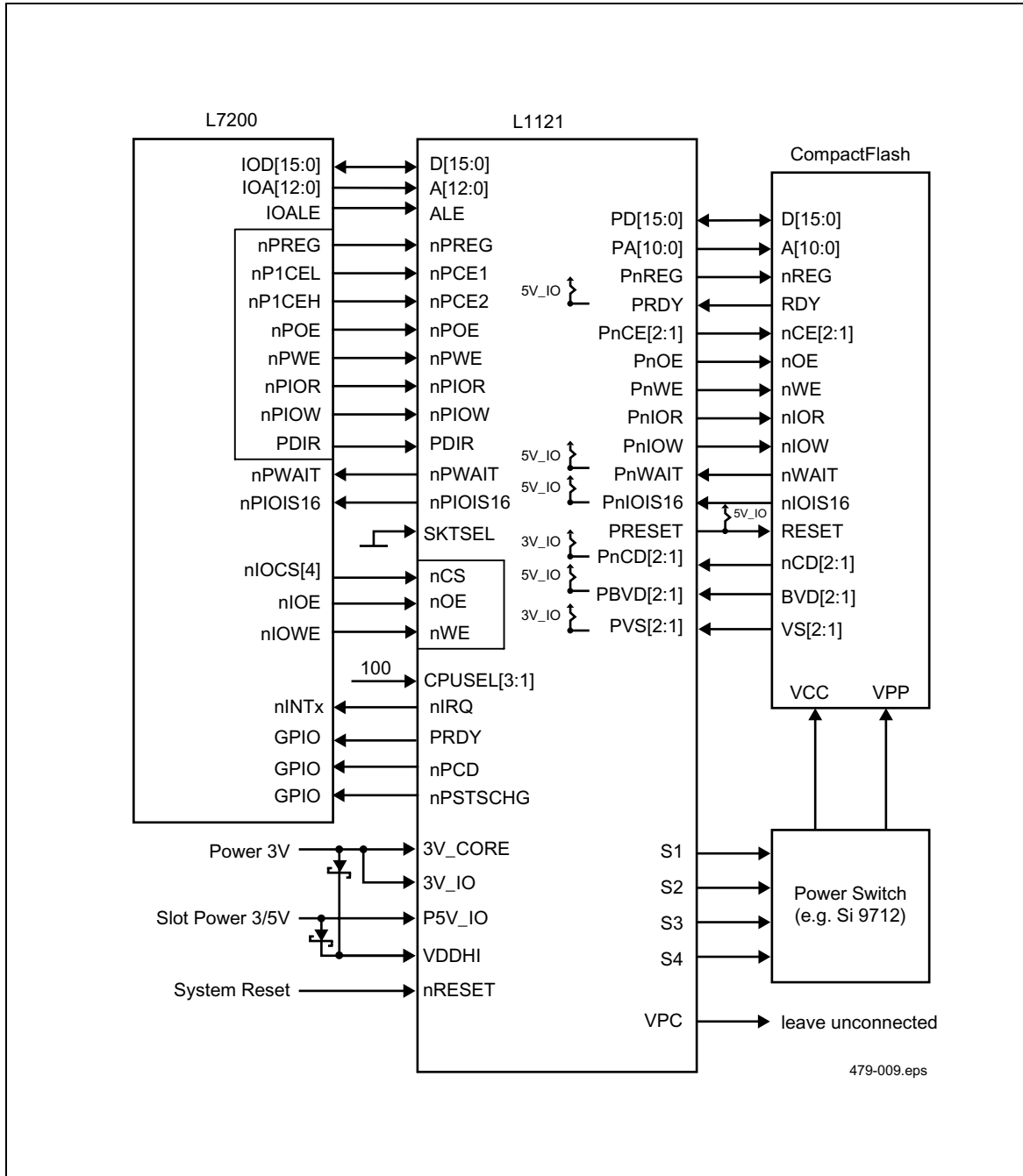
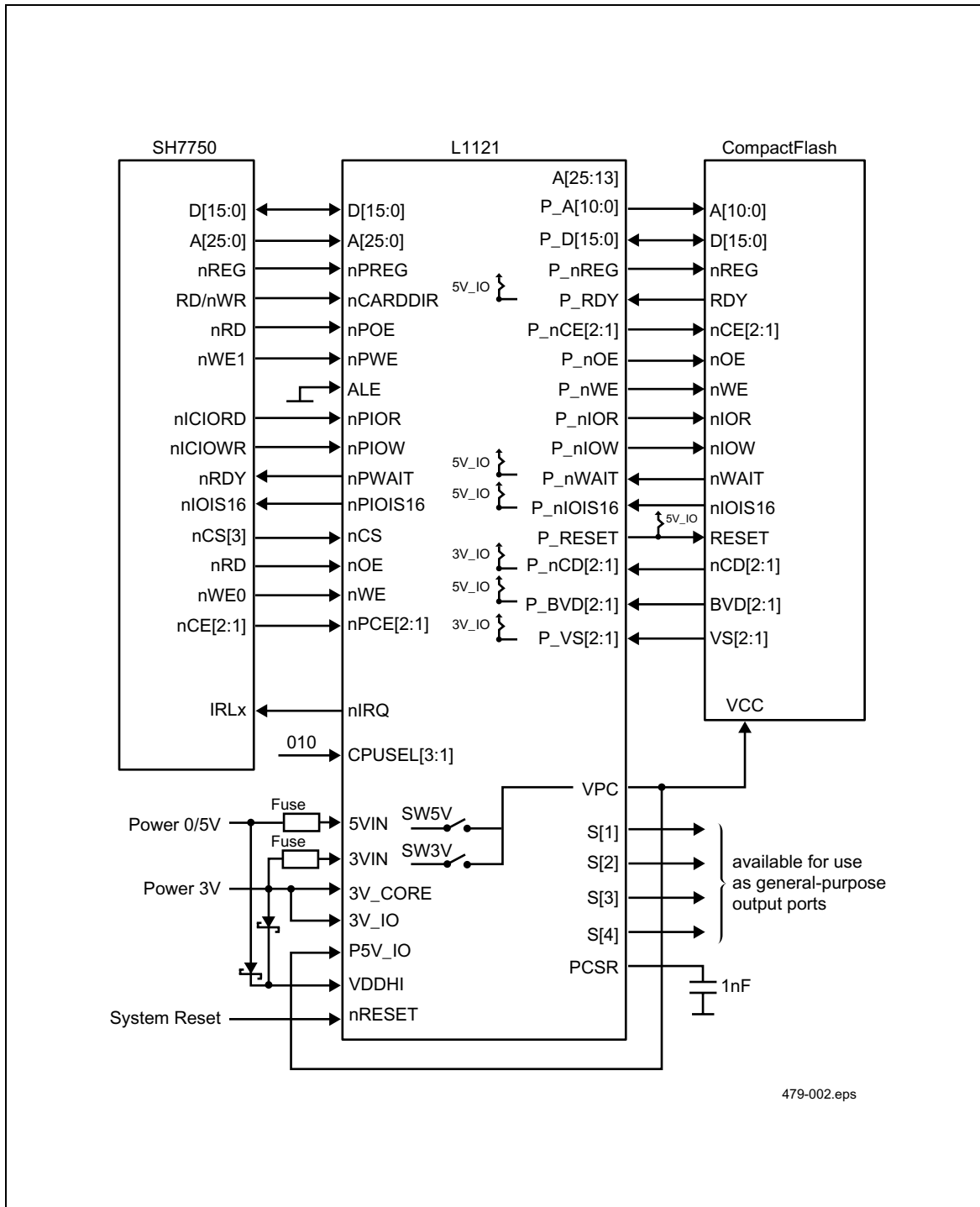


Figure 3. Interface to SH7750 Using On-chip Power Switches for One Slot



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Figure 4. Interface to SA-1100 Using Off-chip Power Switches for One Slot

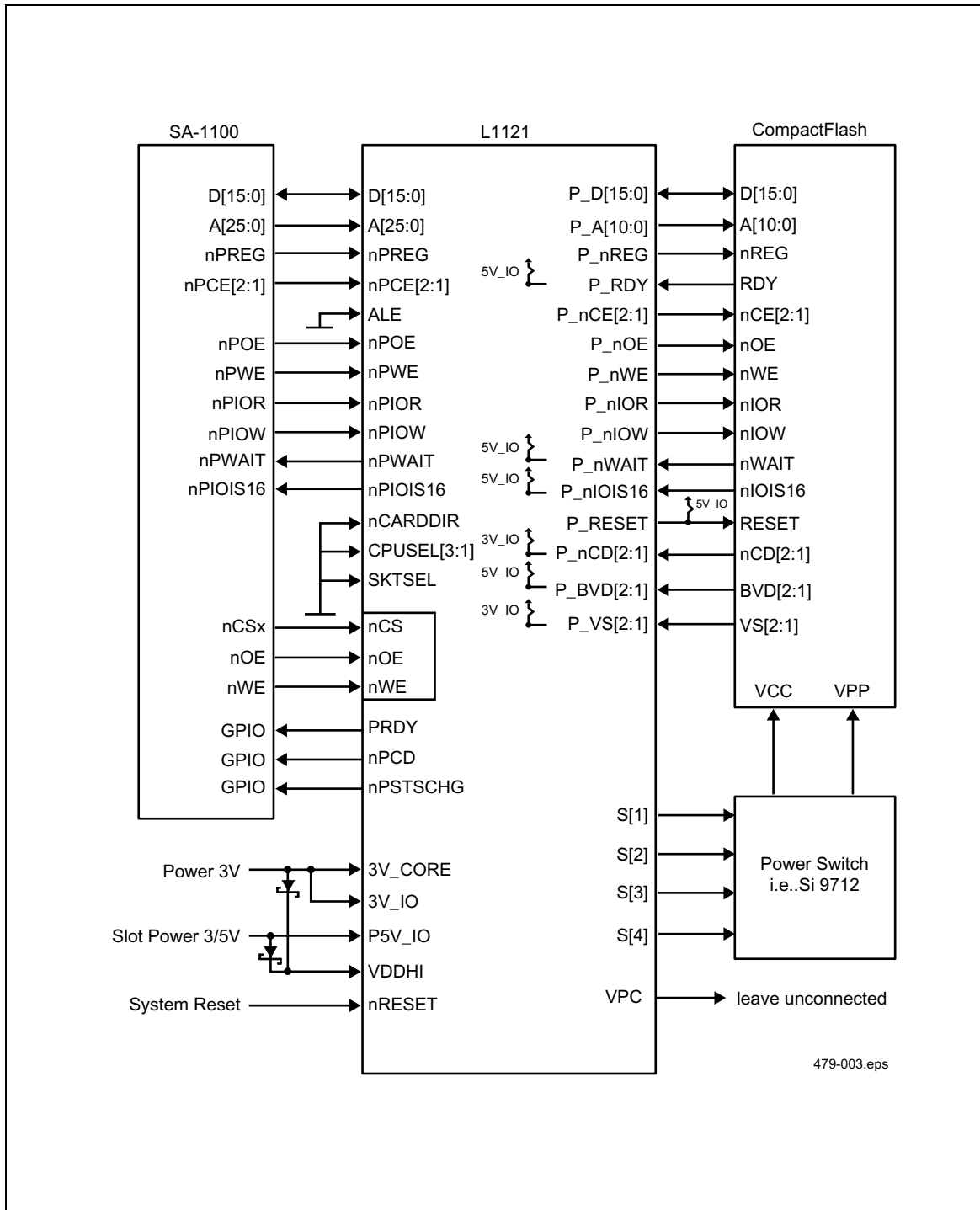


Figure 5. Interface to MPC823 Using On-chip Power Switches for One Slot

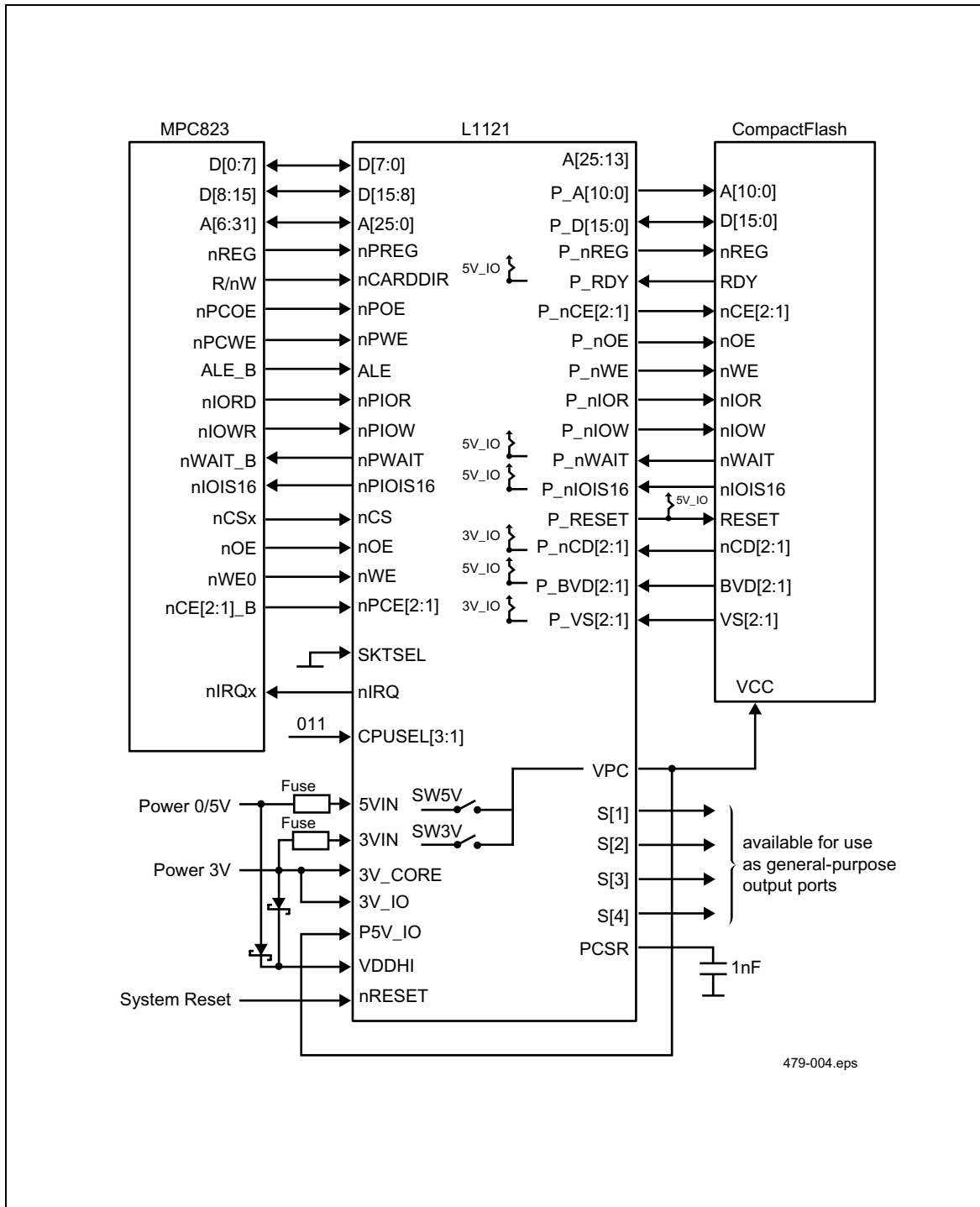
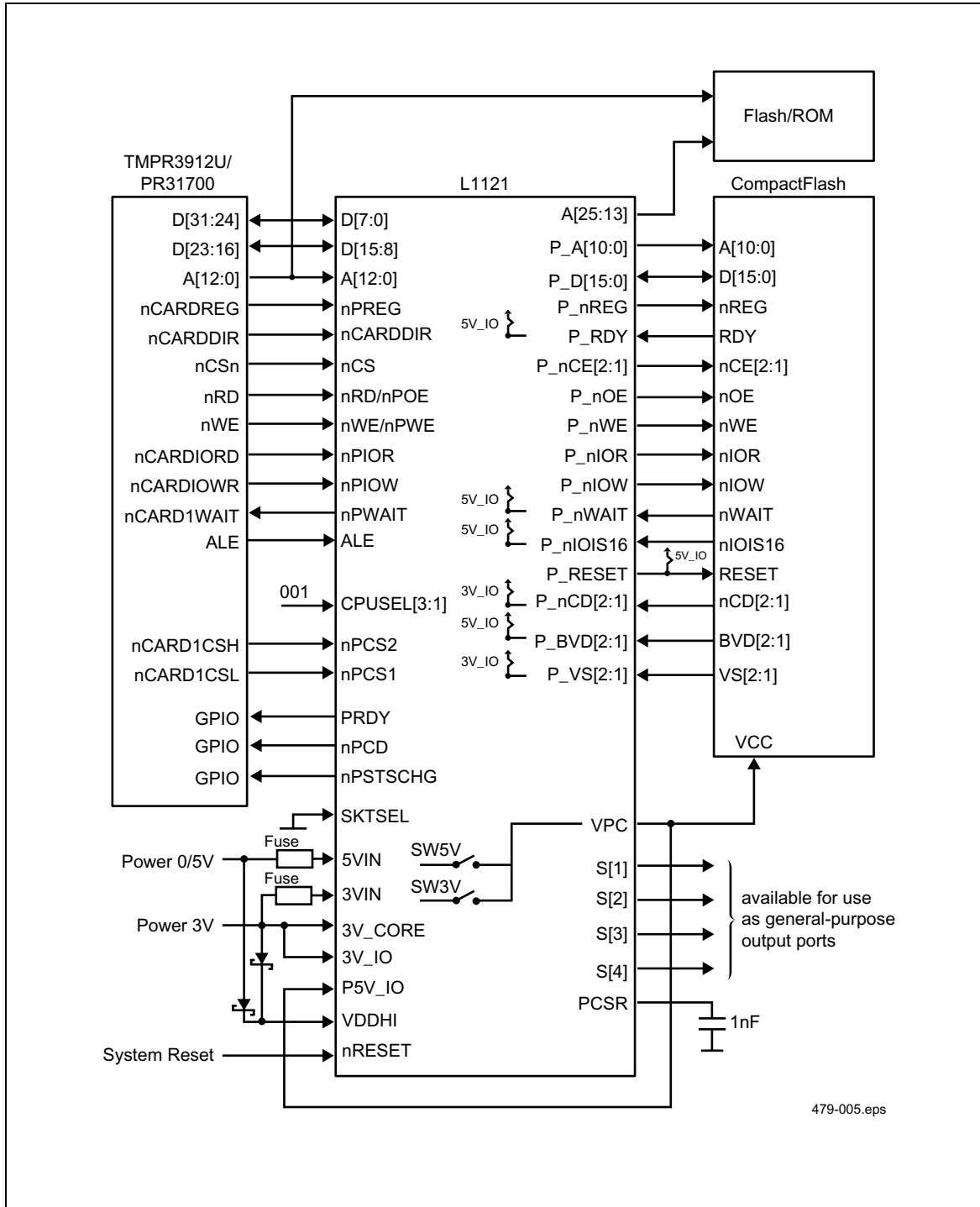


Figure 6. Interface to TMPR3912U/PR31700 Using On-chip Power Switches for One Slot



PIN ASSIGNMENTS

Figure 7 shows the pin assignments for the L1121. Table 1 is an alphanumerical list of the assignments of signals to pins.

Figure 7. L1121 Pin Diagram

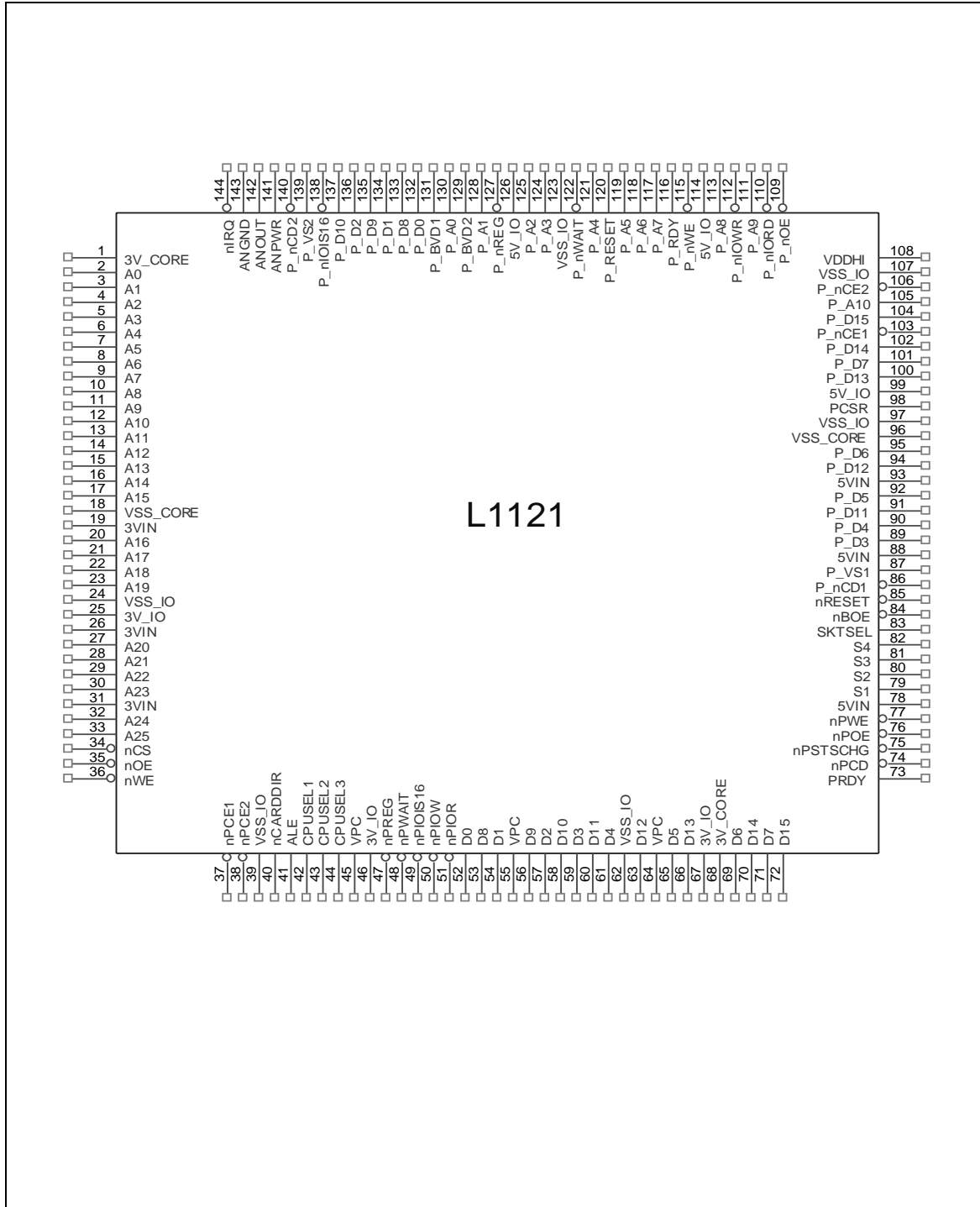


Table 1. Alphanumerical List of L1121 Pin Assignments

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
A0	2	D3	59	P_nCD2	140	P_nWE	115
A1	3	D4	61	P_A0	130	P_RDY	116
A2	4	D5	65	P_A1	128	P_RESET	120
A3	5	D6	69	P_A2	125	P_VS1	87
A4	6	D7	71	P_A3	124	P_VS2	139
A5	7	D8	53	P_A4	121	S1	79
A6	8	D9	56	P_A5	119	S2	80
A7	9	D10	58	P_A6	118	S3	81
A8	10	D11	60	P_A7	117	S4	82
A9	11	D12	63	P_A8	113	SKTSEL	83
A10	12	D13	66	P_A9	111	VDDHI	108
A11	13	D14	70	P_A10	105	VPC	56
A12	14	D15	72	P_D0	132	VPC	64
A13	15	nBOE	84	P_D1	134	VPC	45
A14	16	nCARDDIR	40	P_D2	136	VSS_CORE	18
A15	17	nIRQ	144	P_D3	89	VSS_CORE	96
A16	20	nCS	34	P_D4	90	VSS_IO	24
A17	21	nOE	35	P_D5	92	VSS_IO	39
A18	22	nPCD	74	P_D6	95	VSS_IO	62
A19	23	nPCE1	37	P_D7	101	VSS_IO	97
A20	27	nPCE2	38	P_D8	133	VSS_IO	123
A21	28	nPIOIS16	49	P_D9	135	VSS_IO	107
A22	29	nPIOR	51	P_D10	137	3VIN	26
A23	30	nPIOW	50	P_D11	91	3VIN	19
A24	32	nPOE	76	P_D12	94	3VIN	31
A25	33	nPREG	47	P_D13	100	5VIN	78
ALE	41	nPSTSCHG	75	P_D14	102	5VIN	88
ANGND	143	nPWAIT	48	P_D15	104	5VIN	93
ANOUT	142	nPWE	77	P_nCE1	103	3V_CORE	1
ANPWR	141	nRESET	85	P_nCE2	106	3V_CORE	68
CPUSEL1	42	nWE	36	P_nIOIS16	138	3V_IO	25
CPUSEL2	43	PCSR	98	P_nIOR	110	3V_IO	46
CPUSEL3	44	PRDY	73	P_nIOW	112	3V_IO	67
D0	52	P_BVD1	131	P_nOE	109	5V_IO	99
D1	54	P_BVD2	129	P_nREG	127	5V_IO	114
D2	57	P_nCD1	86	P_nWAIT	122	5V_IO	126

SIGNAL DESCRIPTIONS

Pin Name	Description
CPU Interface (all signals use CMOS levels)	
A[25:13]	CPU Address Bus [25:13]: The upper address signals can be either inputs or outputs as controlled by the CPU type sampled on the CPUSEL[3:1] pins. For CPUs that do not multiplex the address bus, these pins are configured as an input bus for the CPU address. For CPUs that multiplex the address bus, these pins are configured as an unmultiplexed output bus for the upper address bits, which may be used to drive the address inputs of ROM or Flash memory. When used as an output bus, the upper bits of the CPU address A[25:13] are latched on the falling edge of ALE.
A[12:0]	CPU Address Bus [12:0]: The lower address signals are connected to the CPU address bus A[12:0].
ALE	Address Latch Enable: Input used to latch the upper address signals A[25:13]. If the CPU generates this signal, then the upper address is valid when ALE is high and the lower address is valid when ALE is low. The falling edge of this signal latches the upper 13 address bits from A[12:0].
D[15:0]	CPU Data Bus: Bidirectional bus driven by the L1121 when nPCE[2:1] and either nPIOR or nPOE are asserted. For accessing the on-chip PC Card registers, nCS and nOE have to be active.
nCS	Chip Select: Input used with nOE and nWE to read and write the on-chip PC Card registers. A[8:2] are decoded to access the on-chip registers.
nOE	Output Enable: Input used with nCS to read the on-chip PC Card registers.
nWE	Write Enable: Input used with nCS to write to the on-chip PC Card registers.
nIRQ	Interrupt Request: Output used as an interrupt request to the CPU. It is generated from the PC Card signals BVD[2:1], P_RDY, VS[2:1], P_nIOIS16, or P_nCD[2:1]. The polarity of this signal is programmed by the IRQP bit of Command Register 1 (CR1).
CPUSEL[3:1]	CPU Select: Inputs that select the CPU type for controlling the interface protocol. 000 - SA-1100 001 - PR3xxx or TMPR3922U 010 - SH7750 011 - MPC823 100 - L7200 111 - Reserved
SKTSEL	Socket Select: Input that indicates which socket this chip is driving. In a two-socket system with two L1121 chips, SKTSEL has to be tied to VDD for one chip and GND for the other chip. The address signal A8 selects control and status registers in either chip, depending of the state of SKTSEL.
nBOE	Buffer Output Enable: Output used as an output enable control to an external buffer for isolating the A[25:11] from the PC Card address bus. This signal is needed for PC Card support. It is driven high when one of the P_nCD[2:1] signals is high or the SOE bit of Command Register 1 (CR1) is 0.
nCARDDIR	Card Direction: Input asserted by the CPU for reads from a PC Card device. It should be connected to GND when interfacing to a CPU such as the SA-1100 that does not provide a direction control signal. The polarity of this signal is programmed by the DIRP of Command Register 1 (CR1).
nRESET	Reset Input: Input normally connected to the system reset signal. All output signals on the PC Card bus are tristated when nRESET is asserted. Command Register 2 (CR2) is cleared when nRESET is asserted, so the S[4:1] power control outputs are taken low.
Analog Interface	
ANOUT	Analog Output: Output in the range from 0 to ANPWR controlled by the contents of the DAC Register. The output has 2 mA drive capability.

Pin Name	Description
CompactFlash/PC Card CPU Interface (refer to the CPU datasheet for details; all signals use CMOS levels)	
nPCE[2:1]	Card Enable: Input from nPCE[2:1] signals.
nPIOIS16	IO is 16 bit: Output to nPIOIS16 signal.
nPIOR	IO Read: Input from nPIOR signal.
nPIOW	IO Write: Input from nPIOW signal.
nPOE	Output Enable: Input from nPOE signal.
nPREG	REG Select: Input from nPREG signal.
nPWAIT	Wait: Output to nPWAIT.
PRDY	Ready: Output derived from the P_RDY signal from the PC Card device. This signal may be used to generate an interrupt to the CPU, or the nIRQ output may be used. The STOE bit in Command Register 1 (CR1) has to be set, otherwise PRDY is tristated.
nPWE	Write Enable: Input from nPWE signal.
nPSTSCHG	Status Change: Output to a general-purpose I/O port signal. This output is derived from the P_BVD[1] signal from the PC Card device. This signal may be used to generate an interrupt to the CPU, or the nIRQ output may be used. The STOE bit in Command Register 1 (CR1) has to be set, otherwise nPSTSCHG is tristated.
nPCD	Card Detect: Output to a general-purpose I/O port signal. This output is driven low when both P_nCD[2] and P_nCD[1] are low, otherwise it is high. It indicates that a card is inserted. The status of these pins can also be read in the Status Register (SR). This signal may be used to generate an interrupt to the CPU, or the nIRQ output may be used. The STOE bit in Command Register 1 (CR1) has to be set, otherwise nPCD is tristated.
CompactFlash/PC Card Socket Interface (all signals use CMOS levels)	
P_RESET	Reset: Output for resetting the PC Card device. Asserted by setting the RESET bit of Command Register 1 (CR1). A pull-up resistor on P_RESET is required to ensure that the card is reset while nRESET is active.
P_A[10:0]	Address Bus: Address output driven to the PC Card address bus. This bus is tristated when one of the P_nCD[2:1] signals is high or the SOE bit of Command Register 1 (CR1) is clear.
P_D[15:0]	Data Bus: Used to transfer data between the PC Card socket and the CPU. Only 8- and 16-bit operations are supported. In the SA-1100 mode, this bus is driven by the L1121 only when: <ol style="list-style-type: none"> nCE1,2 is asserted and nPIOR and nPOE are not asserted, and P_nCD[2:1] are both low, and SOE bit in Command Register 1 (CR1) is set In all other cases, this bus is tristated. The inputs are protected from drawing current if no card is attached.
P_nREG	nREG: Output to PC Card socket nREG signal. P_nREG is tristated if one of the P_nCD[2:1] signals is high or the SOE bit in Command Register 1 is clear.
P_nCE[2:1]	Card Enable: Output to PC Card socket nCE[2:1] signals. P_nCE[2:1] are tristated if one of the P_nCD[2:1] signals is high or the SOE bit in Command Register 1 is clear.
P_nOE	Output Enable: Output to PC Card socket nOE signal. P_nOE is tristated if one of the P_nCD[2:1] signals is high or the SOE bit in Command Register 1 is clear.
P_nWE	Write Enable: Output to PC Card socket nWE signal. P_nWE is tristated if one of the P_nCD[2:1] signals is high or the SOE bit in Command Register 1 is clear.
P_nIOR	IO Read: Output to PC Card socket nIOR signal. P_nIOR is tristated if one of the P_nCD[2:1] signals is high or the SOE bit in Command Register 1 is clear.
P_nIOW	IO Write: Output to PC Card socket nIOW signal. P_nIOW is tristated if one of the P_nCD[2:1] signals is high or the SOE bit in Command Register 1 is clear.
P_nWAIT	Wait Signal: Input from PC Card socket nWAIT. A weak pull-up resistor to P5V_IO is on-chip.
P_nIOIS16	IO is 16 bit: Input from PC Card socket nIOIS16. A weak pull-up resistor to P5V_IO is on-chip.
P_RDY	Ready/Interrupt Request: Input from PC Card socket RDY/nIRQ signal. A weak pull-up resistor

Pin Name	Description
	to 5V_IO is on-chip.
P_BVD[2:1]	Battery Voltage Detect: Input from PC Card socket battery voltage detect signals BVD[2:1]. A weak pull-up resistor to 5V_IO is on-chip.
P_VS[2:1]	Voltage Sense: Input from PC Card socket voltage sense signals VS[2:1]. A weak pull-up resistor to 3V_IO is on-chip.
P_nCD[2:1]	Card Detect: Input from PC Card Socket card detect signals nCD[2:1]. If one of the P_nCD[2:1] signals is inactive, all PC Card outputs are tristated. A very weak pull-up to 3V_IO is on-chip.
S[4:1]	Power Control Signals: Output control signals to the power switch (e.g. Temic Si9712). S[4:1] are low when nRESET is asserted. These signals are unaffected by the state of P_RESET. They reflect the state of the S[4:1] bits of Command Register 2 (CR2). These outputs are CMOS level. If automatic power off is programmed and either P_nCD[1] or P_nCD[2] is inactive, then the outputs are forced low and remain low until set by software. If S[4:1] are not needed for power control, they may be used as general-purpose output ports.
PCSR	Slew Rate Capacitor: Connect a 1 nF capacitor from this pin to Vss for slew rate control of VPC.
Power Supply Pins	
ANPWR	Analog Power: For the D/A converter.
ANGND	Analog Ground: For the D/A converter.
3V_CORE	VDD: For core power.
3V_IO	VDD: For I/O power.
5V_IO	PC Card I/O Power: It may be 0, 3.3V, or 5V and is connected to the PC Card power if an external power switch is used. If the on-chip power switch is used, this supply is connected to VPC, which may be at 5V or 3V.
3VIN	3V Input: Supply voltage for power switch.
5VIN	5V Input: Supply voltage for power switch.
VPC	PC Card Socket Power: Socket power output from 3V/5V switches.
VDDHI	VDD: This pin has to be at 3V or 5V depending on the socket voltage. See the interface block diagrams.
VSS_CORE	VSS: For core power.
VSS_IO	VSS: For I/O power.

FUNCTIONAL DESCRIPTION

PC Card Interface

The L1121 is designed to provide a glueless interface between LinkUp L7200, Intel SA-1100, Toshiba TMPR3922U, Hitachi SH7750, Motorola MPC823, and Philips PR3xxxx series integrated processors and one CompactFlash or PC Card device. The L1121 buffers the different CPU's PC Card address, data, and control signals, and it directly connects to the PC Card socket interface. The L1121 performs the 3V to 5V and 5V to 3V signal conversions. In addition, L1121 provides status registers for the CPU to monitor the status of the PC Card signals.

Interrupt Controller

The L1121 interrupt controller allows the CPU to handle different interrupt sources from the PC Card device through a single nIRQ pin. It is the responsibility of software to set up the L1121 interrupt registers for proper operation. The PC Card signals P_RDY, P_BVD[2:1], P_VS[2:1], P_nIOIS16, and P_nCD[2:1] are available to the interrupt controller and may generate interrupts.

Any interrupt source can be programmed as level- or edge-triggered. The level of an interrupt source is defined as active low. However, an interrupt source may be defined as rising- or falling-edge sensitive. Interrupts are enabled by setting the corresponding bits in the Interrupt Enable Register (IER).

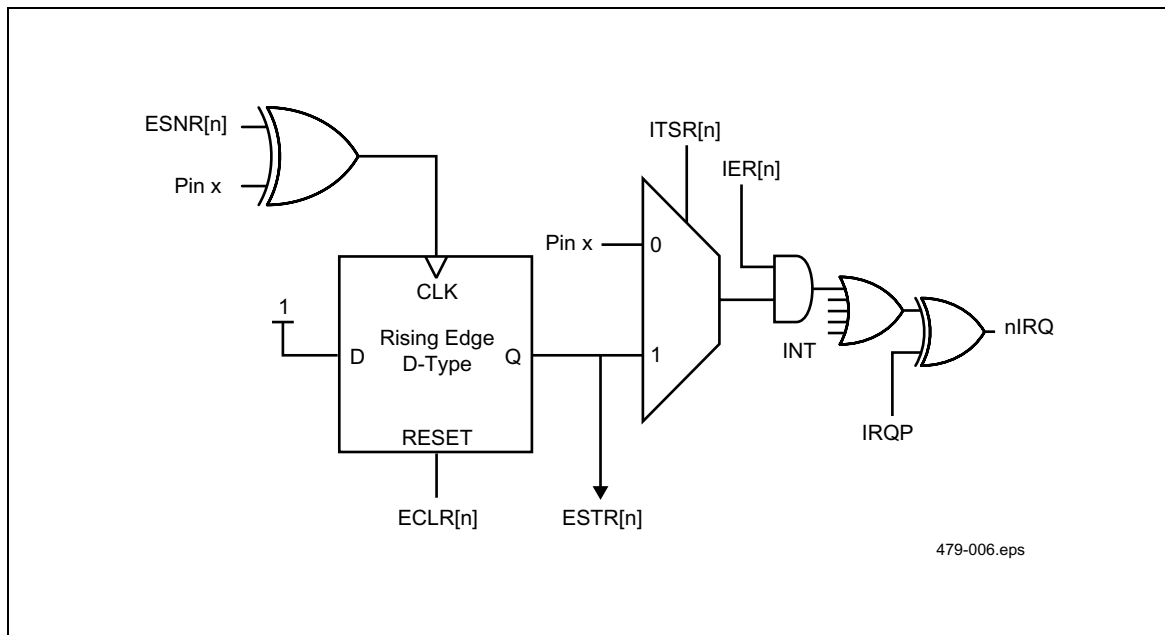
When the CCDIE bit in Command Register 3 (CR3) is set, the card detect interrupts are combined. If the Interrupt Type Select Register (ITSR) is programmed for level-sensitive interrupts and the CCDIE bit is set, then both P_nCD[2:1] signals must be low for an interrupt to be generated. If the ITSr is programmed for falling-edge interrupts and the CCDIE bit is set, both signals P_nCD[2:1] have to transition from high to low for an interrupt to be generated. If the ITSr is programmed for rising-edge interrupts and the CCDIE bit is set, either signal P_nCD[2:1] transitioning from low to high can cause an interrupt.

Four registers are used to program level- and edge-triggering and edge-sensitivity for each pin:

- Interrupt Enable Register (IER)
- Edge Interrupt Sense Register (ESNR)
- Interrupt Type Select Register (ITSr)
- Edge Interrupt Clear Register (ECLR)

Figure 8 shows a conceptual model of the interrupt logic controlled by these registers. The Edge Interrupt Sense Register (ESNR) bits determine the active edge of the corresponding input pin. If a bit is clear and the corresponding interrupt is programmed as edge-triggered, then the interrupt is rising-edge sensitive. If the bit is set, the interrupt is falling-edge sensitive. Once an edge-triggered interrupt is detected, a 1 has to be written to the corresponding bit in the Edge Interrupt Clear Register (ECLR) to clear the interrupt so that subsequent interrupts can be detected. The corresponding bits in the Interrupt Enable Register (IER) should be clear when the ESNR register is programmed, to avoid spurious interrupts. The corresponding bits in the ECLR register should be written with 1 before an interrupt is enabled. The Edge Interrupt Status Register (EISR) indicates whether a particular edge transition has been detected.

Figure 8. Interrupt Logic



When an Interrupt Type Select Register (ITSr) bit is clear, the corresponding interrupt is programmed as level-triggered. The signals from the PC Card pins are passed through to the interrupt logic. When an ITSr bit is set, the corresponding interrupt is programmed as edge-triggered, and the current state of the edge-detection logic is passed to the enable logic.

The Edge Interrupt Clear Register (ECLR) is used to clear specific bits in the Edge Interrupt Status Register (EISR). Writing a 1 to a bit clears the corresponding interrupt. Writing a 0 has no effect.

The eight PC Card pins (see Table 2) have an Interrupt Enable Register bit and an Interrupt Source Register bit associated with them. These registers are used to allow interrupts (level- or edge-triggered) to be passed to the system interrupt controller. The PC Card interrupts are combined and passed to a single nIRQ pin for use by the CPU. It is up to software to read the Interrupt Source Register (ISR) or the Status Register (SR) to determine which pin or pins caused the interrupt. It is also the responsibility of software to set up the appropriate enable bits and clear the interrupt source bits for the interrupt controller to work properly.

Interrupt Register Bit Assignments

The bits in the Interrupt Source Register (ISR), Edge Interrupt Status Register (EISR), Interrupt Enable Register (IER), Edge Interrupt Sense Register (ESNR), Interrupt Type Select Register (ITSR), and Edge Interrupt Clear Register (ECLR) are mapped to interrupt-capable PC Card signals as shown in Table 2.

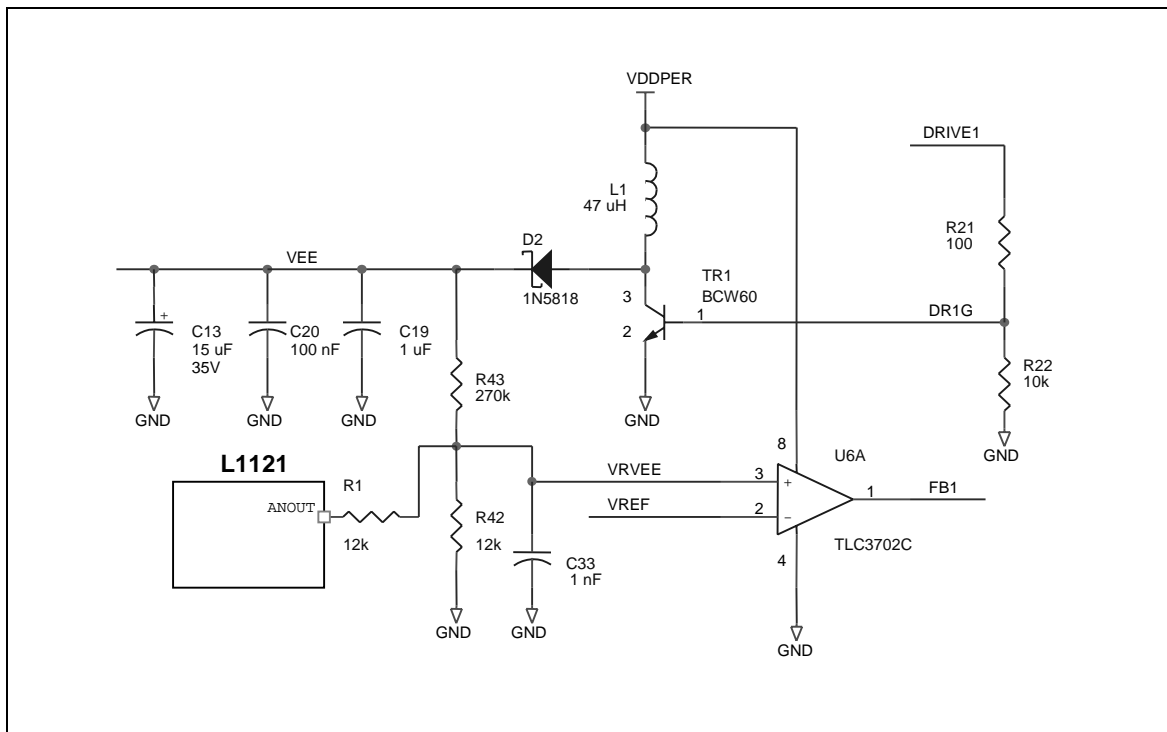
Table 2. Interrupt Register Bit Assignments

Bit	PC Card Signals
0	P_RDY
1	P_BVD[2]
2	P_BVD[1]
3	P_VS[2]
4	P_VS[1]
5	P_nIOIS16
6	P_nCD[2]
7	P_nCD[1]

D/A CONVERTER

The D/A converter is intended for contrast control of an LCD panel. There are three power-down modes available. The DAC output is set to zero voltage during Power On Reset. The output buffer is a rail-to-rail operational amplifier with 2 mA drive capability. A typical application interfacing to the L7200 DC/DC converter is shown in Figure 9. The actual values used for R1, R42, and R43 depend on the target voltage and the voltage range.

Figure 9. Typical D/A Converter Implementation



Power Switch

The on-chip power switch consists of an array of MOSFETs that can be controlled by programming S[3] and S[4] in Command Register 2 (CR2). An external power switch (such as a Temic 9712) can be used if a higher power level is needed. In this case, the S[4:1] outputs reflect the state of the corresponding bits in CR2.

Operation Using On-chip 3V and 5V Power Switch

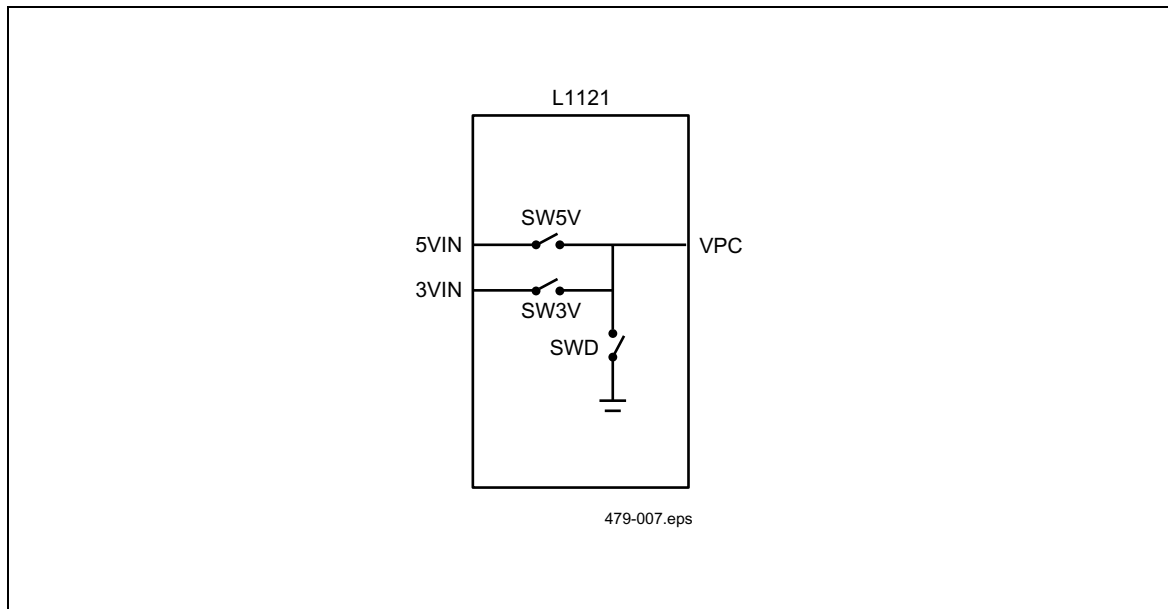
The on-chip MOSFET switches are used to turn on and off the 3V and 5V supplies to the socket. Power is turned on in steps to avoid stressing the power supply and causing spikes. Setting S[3] turns on the 5V Switch (SW5V) and setting S[4] turns on the 3V switch (SW3V). If both S[3] and S[4] are set, then the socket power is off and a small MOSFET SWDischarge (SWD) is turned on to discharge the socket power. The PDCS bit in CR2 shuts off power without regard for S[3] and S[4]. Table 3 summarizes the switch control states as determined by the register bits and the nRESET input.

Table 3. Switch Control States

PDCS	nRESET	S[3]	S[4]	SW3V	SW5V	SWDischarge
1	1	0	0	off	off	on
1	1	0	1	on	off	off
1	1	1	0	off	on	off
1	1	1	1	off	off	on
0	1	X	X	off	off	on
1	0	0	0	off	off	on
0	0	0	0	off	off	on

Asserting the input signal nRESET clears all CR2 register bits, so S[3] and S[4] turn off the power to the socket after nRESET is asserted. A clear PDCS bit also turns off power to the socket. Figure 10 shows the operation of the power switches.

Figure 10. On-chip Power Switches



SOFTWARE INTERFACE

The L1121 contains eighteen 8-bit registers. The read-only registers are accessed when nCS and nOE signals are active. Addresses A[8:0] select the appropriate register as defined in Table 4. The read/write registers are accessed by asserting nCS simultaneously with nOE or nWE. Two L1121 chips can be used to support two sockets. The L1121 chip uses the SKTSEL input pin to determine which address range is assigned to its registers. If SKTSEL is low, then the registers are assigned to addresses with A[8] = 0. If SKTSEL is high, then the registers are assigned to addresses with A[8] = 1. For systems with two L1121 chips, the CPU will see two sets of registers, one at address A[8:0] = 0xx and the other at address A[8:0] = 1xx.

Table 4. Register Map

Memory Map Address	Register	Function	Type
x00	IDR1	ID Register 1	read only
x04	IDR2	ID Register 2	read only
x08	IDR3	ID Register 3	read only
x0C	IDR4	ID Register 4	read only
x10	SR	Status Register	read only
x14	ISR	Interrupt Source Register	read only
x18	EISR	Edge Interrupt Status Register	read only
x1C	reserved		
x20	reserved		
x24	CR1	Command Register 1	read/write
x28	CR2	Command Register 2	read/write
x2C	IER	Interrupt Enable Register	read/write
x30	ESNR	Edge Interrupt Sense Register	read/write
x34	ITSR	Interrupt Type Select Register	read/write
x38	ECLR	Edge Interrupt Clear Register	read/write
x3C	CR3	Command Register 3	read/write
x40	DACCR	DAC Control Register	read/write
x44	DACDR	DAC Data Register	read/write

Note: x = 0 for SKTSEL low; x = 1 for SKTSEL high

ID Register 1 (IDR1)

Bit	7	6	5	4	3	2	1	0
Name	IDR1[7]	IDR1[6]	IDR1[5]	IDR1[4]	IDR1[3]	IDR1[2]	IDR1[1]	IDR1[0]

This ID is reserved for LinkUp Systems Corporation internal use only. IDR1 reads as 0x01.

ID Register 2 (IDR2)

Bit	7	6	5	4	3	2	1	0
Name	IDR2[7]	IDR2[6]	IDR2[5]	IDR2[4]	IDR2[3]	IDR2[2]	IDR2[1]	IDR2[0]

This ID is reserved for LinkUp Systems Corporation internal use only. IDR2 reads as 0x10.

ID Register 3 (IDR3)

Bit	7	6	5	4	3	2	1	0
Name	IDR3[7]	IDR3[6]	IDR3[5]	IDR3[4]	IDR3[3]	IDR3[2]	IDR3[1]	IDR3[0]

This ID is reserved for LinkUp Systems Corporation internal use only. IDR3 reads as 0x12.

ID Register 4 (IDR4)

Bit	7	6	5	4	3	2	1	0
Name	IDR4[7]	IDR4[6]	IDR4[5]	IDR4[4]	IDR4[3]	IDR4[2]	IDR4[1]	IDR4[0]

This ID is for LinkUp Systems Corporation internal use only. IDR4 reads as 0x01.

Status Register (SR)

Bit	7	6	5	4	3	2	1	0
Name	CD1	CD2	WRP	VS1	VS2	BVD1	BVD2	RDY

Bit	Name	Description
0	RDY	P_RDY status: Indicates the state on the P_RDY pin.
1	BVD2	Battery Voltage Detect 2 status: Indicates the state on the P_BVD[2] pin.
2	BVD1	Battery Voltage Detect 1 status: Indicates the state on the P_BVD[1] pin.
3	VS2	Voltage Sense 2 status: Indicates the state on the P_VS[2] pin.
4	VS1	Voltage Sense 1 status: Indicates the state on the P_VS[1] pin.
5	WRP	Write Protect bit: Indicates the state on the P_nOIS16 pin.
6	CD2	Card Detect 2: Indicates the state on the P_nCD[2] pin.
7	CD1	Card Detect 1: Indicates the state on the P_nCD[1] pin.

Note: The default value for this register is determined by the states on the corresponding I/O pins.

Interrupt Source Register (ISR)

Bit	7	6	5	4	3	2	1	0
Name	ISR[7]	ISR[6]	ISR[5]	ISR[4]	ISR[3]	ISR[2]	ISR[1]	ISR[0]

This register contains the logical AND of the PC Card interrupt source (edge or level) and the corresponding bit in the IER register. This register is cleared by asserting nRESET. Table 5 shows the mapping of interrupt sources to register bits.

Table 5. Interrupt Register Bit Assignments

Bit	PC Card Signals
0	P_RDY
1	P_BVD[2]
2	P_BVD[1]
3	P_VS[2]
4	P_VS[1]
5	P_nIOIS16
6	P_nCD[2]
7	P_nCD[1]

Edge Interrupt Status Register (EISR)

Bit	7	6	5	4	3	2	1	0
Name	EISR[7]	EISR[6]	EISR[5]	EISR[4]	EISR[3]	EISR[2]	EISR[1]	EISR[0]

This register contains the current state of the edge detection logic. Table 5 shows the mapping of interrupt sources to register bits. It indicates whether a particular edge transition has occurred. This register is cleared by asserting nRESET.

Command Register 1 (CR1)

Bit	7	6	5	4	3	2	1	0
Name	SOE	Reserved	APOE	RESET	STOE	BIG	IRQP	DIRP

This register is cleared when nRESET is active.

Bit	Name	Description
0	DIRP	nCARDDIR Input Pin Polarity: Determines the polarity of nCARDDIR for a CPU read. 0 - Low on nCARDDIR means a read cycle is in progress 1 - High on nCARDDIR means a read cycle is in progress
1	IRQP	nIRQ Output Pin Polarity: Determines the polarity of the nIRQ interrupt request. 0 - Low on nIRQ means an interrupt is pending. 1 - High on nIRQ means an interrupt is pending.
2	BIG	Endian Select: If this bit is set, the card is read in big-endian mode. D[7:0] is mapped to P_D[15:8], and D[15:8] is mapped to P_D[7:0]. If this bit is clear (default), the card is read in little-endian mode. D[7:0] is mapped to P_D[7:0], and D[15:8] is mapped to P_D[15:8]. In either mode, nPxCE[2:1] is mapped to P_nCE[2:1].
3	STOE	Status Signal Output Enable: If this bit is set, the output buffers of the status signals PSTSCHG, PRDY, and nPCD are driven. If clear, these signals are tristated.
4	RESET	Software Reset: This bit drives the P_RESET output. If set, the P_RESET output is high.
5	APOE	Automatic Power Off Enable: If this bit is set, S[4:1] is automatically cleared when either P_nCD[1] or P_nCD[2] become active high, effectively turning off the power to the slot. S[4:1] does not regain its original state if P_nCD[1] and P_nCD[2] should become active.
6	Reserved	
7	SOE	PC Card Socket Signal Output Driver Enable: The socket signals will not be driven unless this bit is set. This bit controls the following output I/O pins: P_RESET, P_A[10:0], P_D[15:0], P_nREG, P_nCE[2:1], P_nOE, P_nWE, P_nIOR, and P_nIOW.

Command Register 2 (CR2)

Bit	7	6	5	4	3	2	1	0
Name	PDCS	RTRIM	RTRIM	DISS	S[4]	S[3]	S[2]	S[1]

This register is cleared when nRESET is active.

Bit	Name	Description
3:0	S[4:1]	Voltage Control: These register bits are driven out to the I/O pins S[4:1].
4	DISS	Disable Over-current Protection: Controls the on-chip switch. 0 - Enable over-current protection 1 - Disable over-current protection
6:5	RTRIM	Trim Register: Value will be determined at device characterization.
7	PDCS	Power Down Current Source: This bit, when clear, turns off the on-chip power switch. Default is clear.

Interrupt Enable Register (IER)

Bit	7	6	5	4	3	2	1	0
Name	IER[7]	IER[6]	IER[5]	IER[4]	IER[3]	IER[2]	IER[1]	IER[0]

Any set bit in this register enables an interrupt by the corresponding pin. Table 5 shows the mapping of interrupt sources to register bits. This register is cleared when nRESET is active.

Edge Interrupt Sense Register (ESNR)

Bit	7	6	5	4	3	2	1	0
Name	ESNR[7]	ESNR[6]	ESNR[5]	ESNR[4]	ESNR[3]	ESNR[2]	ESNR[1]	ESNR[0]

If an interrupt is programmed to be edge-triggered, clearing the corresponding bit in this register selects rising-edge sensitivity. Setting the bit selects falling-edge sensitivity. Table 5 shows the mapping of interrupt sources to register bits. Writes to this register may generate spurious interrupts if the interrupt is also enabled in the Interrupt Enable Register (IER). This register is cleared when nRESET is active.

Interrupt Type Select Register (ITSR)

Bit	7	6	5	4	3	2	1	0
Name	ITSR[7]	ITSR[6]	ITSR[5]	ITSR[4]	ITSR[3]	ITSR[2]	ITSR[1]	ITSR[0]

These bits select whether an interrupt is level- or edge-triggered. Table 5 shows the mapping of interrupt sources to register bits. If the corresponding bit is clear, the interrupt is level-triggered. If the bit is set, the interrupt is edge-sensitive. This register is cleared when nRESET is active.

Edge Interrupt Clear Register (ECLR)

Bit	7	6	5	4	3	2	1	0
Name	ECLR[7]	ECLR[6]	ECLR[5]	ECLR[4]	ECLR[3]	ECLR[2]	ECLR[1]	ECLR[0]

Writing a 1 to any bit clears the corresponding edge-detection latch. Writing 0 has no effect. Table 5 shows the mapping of interrupt sources to register bits. Reading from this register returns undefined data. This register is cleared when nRESET is active.

Command Register 3 (CR3)

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	MIO	CCDIE	WIRQE	WOR16E	WORWE

This register is cleared when nRESET is active.

Bit	Name	Description
0	WORWE	Wire OR nPWAIT Enable: If this bit is set, the nPWAIT I/O pin acts as an open-drain output. This allows wire-OR use of this signal. If this bit is clear, the nPWAIT I/O pin will be a normal output pin.
1	WOR16E	Wire OR nPIOIS16 Enable: If this bit is set, the nPWAIT I/O pin acts as an open-drain output. This allows wire-OR use of this signal. If this bit is clear, the nPIOIS16 I/O pin will be a normal output pin.
2	WIRQE	Wire OR nIRQ Enable: If this bit is set, the nPWAIT I/O pin acts as an open-drain output. This allows wire-OR use of this signal. If this bit is clear, the nIRQ I/O pin will be a normal output pin.
3	CCDIE	Combine Card Detect Interrupt Enable: If this bit is set and the card detect interrupts are programmed as level-triggered, both P_nCD[2:1] signals must be low for an interrupt to occur on nIRQ. If programmed as edge-triggered and falling-edge sensitive, both P_nCD[2] and P_nCD[1] have to transition low to cause an interrupt. If programmed as edge-triggered and rising-edge sensitive, either P_nCD[2] or P_nCD[1] transitioning high causes an interrupt. If this bit is clear, then either P_nCD[2] or P_nCD[1] can cause an interrupt independently of each other.
4	MIO	Memory or I/O: If this bit is set, then P_nIOIS16 signal is WP. Set this bit for memory-only cards. If MIO is clear, then P_nIOIS16 may be activated by the card to indicate a 16-bit transaction.
7:5	Reserved	

DAC Control Register (DACCR)

Bit	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PDOWN[1]	PDOWN[0]

This register is cleared when nRESET is active

PDOWN[1]	PDOWN[0]	Operation
0	0	Normal operation
0	1	7 k Ω to GND on ANOUT
1	0	300 k Ω to GND on ANOUT
1	1	ANOUT is tristated

DAC Data Register (DACDR)

Bit	7	6	5	4	3	2	1	0
Name	DACDR[7]	DACDR[6]	DACDR[5]	DACDR[4]	DACDR[3]	DACDR[2]	DACDR[1]	DACDR[0]

Values written to this 8-bit read/write register are converted by the DAC to a voltage level in the range of ANGND and ANPWR. Bit 7 is the MSB and bit 0 is the LSB. This register is cleared when nRESET is active.

ABSOLUTE MAXIMUM RATINGS**Table 6. Absolute Maximum Ratings**

Parameter	Rating
Absolute Temperature under Bias	-55°C to +125°C
Storage temperature	-65°C to +150°C
Junction Temperature	+125°C
Lead Temperature (10 seconds)	+275°C
Supply voltage to Ground	-0.5V to +7.0V
DC Input Voltage	-0.5 to 5.5V Max
DC Output Current	± 10 mA
I _{OUT} VPC	1A
DC Input Current	-10 μA to 10 μA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES**Table 7. Operating Ranges**

Parameter	Rating
Ambient Temperature (T _A)	0°C to +70°C
Supply Voltage (V _{CC})	3.3V ± 10%
Maximum input voltage (V _{in})	5.25V
PCSR Load Capacitor	1 nF
I _{OUT} VPC	0.5A max
V _{PC} Load Capacitance	150 μF max

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

Conditions: V_{3V_CORE} , $V_{3V_IO} = 3.3V \pm 10\%$; $V_{5V_IO} = 5V \pm 5\%$; $V_{SS} = 0V$; Ambient Temperature $T_A = 0^\circ C$ to $70^\circ C$.

Table 8. DC Characteristics

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{ihc}	Input High Voltage CMOS	$0.7 \times V_{cc}$	$V_{cc} + 0.3V$	V	
V_{ilc}	Input Low Voltage CMOS	-0.3V	$0.2 \times V_{cc}$	V	
V_{ohc}	Output High Voltage CMOS	$V_{cc} - 1.0$		V	$I_{oh} = -1$ mA
V_{olc}	Output Low Voltage CMOS		0.4	V	$I_{ol} = 2$ mA
V_{iht}	Input High Voltage TTL	2.0	$V_{cc} + 0.3V$	V	
V_{ilt}	Input Low Voltage TTL		0.8	V	
V_{oht}	Output High Voltage TTL	2.4		V	$I_{oh} = -2$ mA
V_{olt}	Output Low Voltage TTL		0.4	V	$I_{ol} = 2$ mA
I_{in}	Input Leakage Current	-10	+10	μA	$V_{in} = V_{cc}$ or V_{ss}
I_{oh}	Output High Current	-2		mA	Respective Slot $V_{cc} = 3.0V$
I_{oz}	Output Tristate Leakage Current	-10	+10	μA	$V_{out} = V_{cc}$ or V_{ss}
C_{in}	Input Capacitance		10	pF	
C_{out}	Output Capacitance		10	pF	
I_{3V_CORE}	Operating Current		5	mA	No loads
I_{3V_IO}	Operating Current		5	mA	No loads
I_{5V_IO}	Operating Current		5	mA	No loads
I_{VDDHI}	Operating Current		2	mA	No loads
I_{PU}	Pullup Current		30	μA	$5V_IO = 5.25V$
I_{CDPU}	Pullup Current CD[2:1]		10	μA	
$I_{cc\ stby}$	Standby Current		10	μA	Any supply

Table 9. 5V Switch (SW5V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
R_{ON}	On-Resistance	$I = 500$ mA		400	TBD	$m\Omega$
I_{OFF}	Off Current	$5VIN = 5.5V$ $VPC = 0V$			5	μA
t_{SW3}	Rise Time		5	10	15	ms

Table 10. 3V Switch (SW3V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
R_{ON}	On-Resistance	$I = 500$ mA		400	TBD	$m\Omega$
I_{OFF}	Off Current	$3VIN = 3.6V$ $VPC = 0V$			5	μA
t_{SW3}	Rise Time		5	10	15	ms

Table 11. Discharge Switch (SWD)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
R _{ON}	On-Resistance	I = 2 mA			400	Ω

AC CHARACTERISTICS

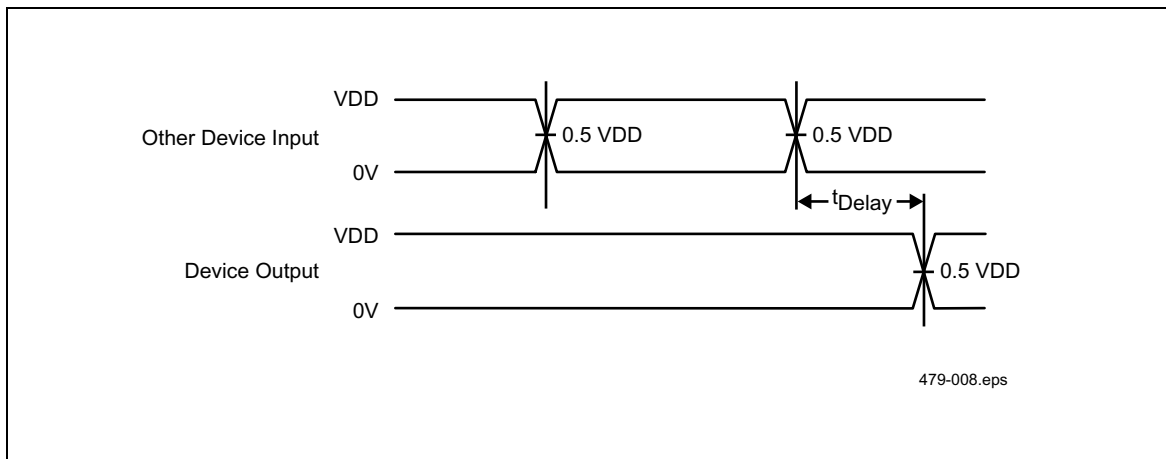
Operating Conditions: V_{3V_CORE}, V_{3V_IO} = 3.3V ± 10%; V_{5V_IO} = 5V ± 5%; T_A = 0°C to 70°C.

Table 12. AC Characteristics

Symbol	Parameter	Min.	Max.	Units	Conditions
t _{prop}	Propagation Delay		35	ns	Any input to output, 5V _{IO} = 5.0V
t _{prop}	Propagation Delay		35	ns	A[25:13] from A[12:0]
t _{rise}	Rise Time		20	ns	Any socket signal at 50 pF load
t _{fall}	Fall Time		15	ns	Any socket signal at 50 pF load
t _{setup}	Data Setup time to nWE high	10		ns	PC Card register write
t _{hold}	Data Hold time from nWE high	2		ns	PC Card register write
t _{Enable}	Output enable		15		Any socket output active from enable

SWITCHING TEST WAVEFORM

All timings are measured at 0.5 VDD (VDD may be 5V_{IO}, 3V_{CORE}, or 3V_{IO}), as shown in Figure 11. For additional capacitive loading, add 0.2 ns for every pF.

Figure 11. Switching Test Waveform


8-BIT DAC SPECIFICATION

Table 13. DAC Characteristics

Parameter	Min.	Typ.	Max.	Units	Conditions/Notes
Resolution	8			bits	
Differential Nonlinearity			±0.5	LSB	
Zero Code Error		+0.5	+4.5	LSB	
Full-Scale Error		+0.5	-3.5	LSB	
Gain Error			±1.25	% of FSR	
Zero Code Error Drift		-20		μV/°C	
Output Voltage Range	0		ANPWR	V	
Output Voltage Settling Time		4	6	μs	
Slew Rate		1		V/μs	
DC Output Impedance		500		Ω	
Short Circuit Current		20		mA	
Power-Up Time		5		μs	
ANPWR	3.0	3.3	3.6	V	

PIN CHARACTERISTICS

This section describes each of the L1121 pins and its characteristics. This is in addition to the Signal Descriptions, with an emphasis on the electrical characteristics. The symbols used are shown in Table 14.

Table 14. Signal Type Symbols

Symbol	Signal Type
N	Active low signal
I/O	Bidirectional
I/OZC	I/O with output tristateable, CMOS
I/OZT	I/O with output tristateable, TTL
IC	Input CMOS
IS	Input with Schmitt trigger
IT	Input TTL
OD	Open-drain output
OC	Output CMOS
OZT	Output tristateable, TTL
OA	Analog output
PU	Pullup resistor on-chip

5V Tolerance

All CompactFlash/PC Card inputs are 5V tolerant. These inputs will tolerate 5V input levels provided the $V_{5V_{IO}}$ voltage is 5V. The current flow to the power plane under this condition is very low. VDDHI must be at the highest voltage of either 3V or 5V. Use two Schottky diodes as shown in the interface circuit schematics between the power sources and the V_{DDHI} pin.

Power Planes

The L1121 device has four power planes as listed in Table 15.

Table 15. Power Plane Symbols

Symbol	Description	Name
S	3.3V supply; same as the CPU input output plane	3V_IO
P	CompactFlash/PC Card slot power, either 3.3V, 5V, or off	5V_IO
C	Core Voltage, this plane drives the on-chip core logic	3V_CORE
A	Analog supply for the D/A converter	ANPWR

PIN FUNCTION
Table 16. Pin Function Descriptions

Signal Name	Pin Type	5V Tolerance	Power Plane	Drive (mA)	Comments
D[15:0]	I/OZC	No	S	4	
A[12:0]	IC	No	S		
A[25:13]	I/OZC	No	S	4	
ALE	IC	No	S		Connect to ground for SA-1100
nRESET	IC	No	S		
nOE	IC	No	S		
nWE	IC	No	S		
nCS	IC	No	S		
nCARDDIR	IC	No	S		
CPUSEL[3:1]	IC	No	S		
nPIOR	IC	No	S		
nPIOW	IC	No	S		
nPCE[2:1]	IC	No	S		
nPIOIS16	OZC	No	S	2	
nPOE	IC	No	S		
nPREG	IC	No	S		
nPWAIT	OZC	No	S	2	
nPWE	IC	No	S		
nPSTSCHG	OZC	No	S	2	Connect to GPIO/Interrupt
nPCD	OZC	No	S	2	Connect to GPIO/Interrupt
nIRQ	OZC	No	S	2	Connect to GPIO/Interrupt
PRDY	OZC	No	S	2	Connect to GPIO/Interrupt
P_D[15:0]	I/OZT	Yes	P	2	
P_A[10:0]	OZT	Yes	P	2	
P_nCD[2:1]	ICPU	No	S		
P_nCE[2:1]	OZT	Yes	P	2	
P_nIOIS16	ITPU	Yes	P		
P_nIOR	OZT	Yes	P	2	
P_nIOW	OZT	Yes	P	2	
P_nOE	OZT	Yes	P	2	

Signal Name	Pin Type	5V Tolerance	Power Plane	Drive (mA)	Comments
P_nREG	OZT	Yes	P	2	
P_nWE	OZT	Yes	P	2	
P_nWAIT	ITPU	Yes	P		
P_RESET	OZT	Yes	P	2	External pull-up resistor required
P_BVD[2:1]	ITPU	Yes	P		
P_RDY	ITPU	Yes	P		
P_VS[2:1]	IPU	No	S		
SKTSEL	IC	No	S		
S[4:1]	OC	No	S	4	
ANOUT	OA	No	A	2	
nBOE	OC	No	S	2	

Table 17. Power and Ground Pin Function Descriptions

Name	Description
ANPWR	Analog power supply for DAC circuitry.
ANGND	Analog ground reference for DAC circuitry.
3V_CORE	3.3V power supply for internal core logic.
3V_IO	Power supply for 3.3V I/O power plane.
5V_IO	Power supply for CompactFlash/PC Card power plane.
3VIN	3.3V power supply source to 3V switch.
5VIN	5.0V power supply source to 5V switch.
VPC	Switch-controlled power supply output.
VDDHI	The highest power supply voltage.
VSS_CORE	The ground reference for internal core logic.
VSS_IO	The ground reference for I/O pad ring.

CPU INTERCONNECTION
Table 18. Connections Between L1121 and Supported CPU Types

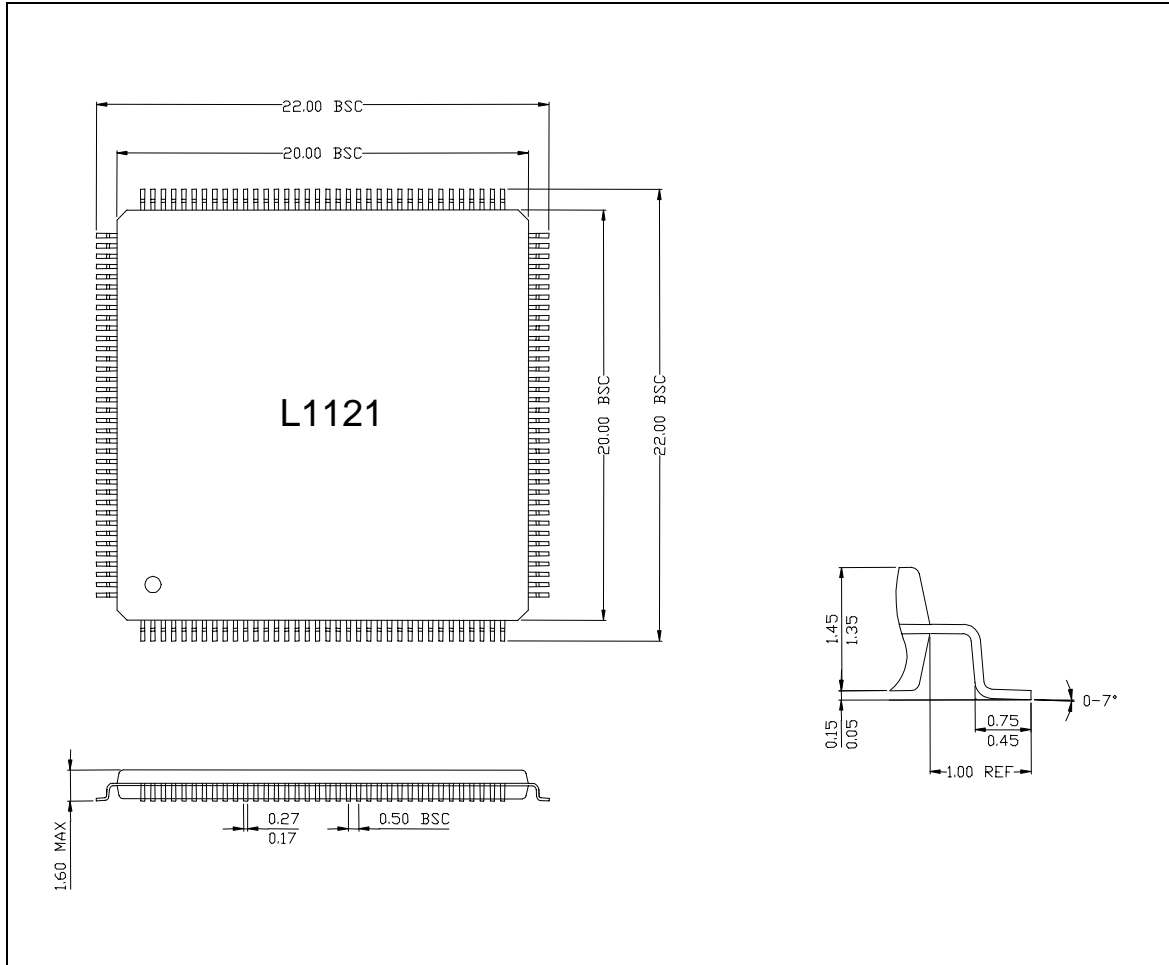
L1121	L7200	SH7750	MPC823	TMPR392U/ PR3xxxx	SA-1100
D[15:0]	IOD[15:0]	D[15:0]	D[8:15], D[0:7]	D[23:31]	D[15:0]
A[12:0]	IOA[12:0]	A[12:0]	A[19:31]	A[12:0]	A[12:0]
A[25:13]	Not Used	A[25:13]	A[6:18]	Not Used	A[25:13]
ALE	IOALE	GND	ALE_B	ALE	PSKTSEL
nRESET	System Reset	System Reset	System Reset	System Reset	System Reset
nOE	nIOE	nRD	nOE	nRD	nOE
nWE	nIOWE	nWE0	nWE0	nWE	nWE
nCS	nIOCS[4]	nCSx	nCSx	nCSx	nCSx
nCARDDIR	PDIR	RD/nWR	R/nW	nCARDDIR	GND
PRDY	GPIO *2	Port[x] *2	RDY *2	GPIO *2	GPIO
nPIOR	nPIOR	nCIORD	nIORD	nCARDIORD	nPIOR
nPIOW	nPIOW	nCIOWR	nIOWR	nCARDIOWR	nPIOW
nPCE[2:1]	nP1CEL, nP1CEH	nCE[2:1]x	nCEx_B	NCARDxCSL, NCARDxCSH	nPCE[2:1]
nPIOIS16	nPIOIS16	nIOIS16	nIOIS16_B	Not Used	nPIOIS16
nPOE	nPOE	nRD	nPCOE	nRD	nPOE
nPREG	nPREG	nREG	nREG	nCARDREG	nPREG
nPWAIT	nPWAIT	nRDY	nWAIT_B	nCARDxWAIT	nPWAIT
nPWE	nPWE	nWE1	nPCWE	nWE	nPWE
nPSTSCHG	GPIO[x] *2	PORT[x] *2	BVD2_B *2	GPIO[x] *2	GPIO[x] *2
nPCD	GPIO[x] *2	PORT[x] *2	CD1_B *2	GPIO[x] *2	GPIO[x] *2
nIRQ	nINT[x] *1	PORT[x] *1	nIRQ7 *1	GPIO[x] *1	GPIO[x] *1
CPUSEL[3:1]	100	010	011	001	000

Note *1: Connection is optional if this pin is connected to an interrupt-capable CPU pin. Then nPCD, nPSTSCHG, and PRDY do not need to be connected to the CPU.

Note *2: These pins do not need to be used by the CPU if nIRQ is used.

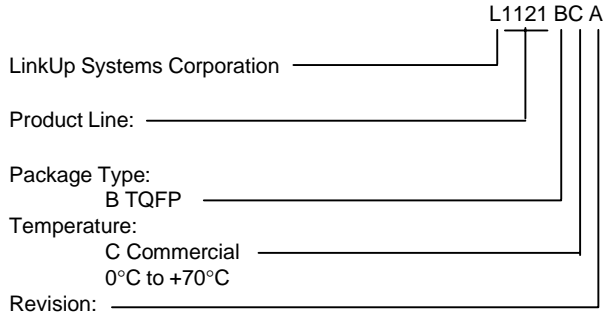
PACKAGE DIAGRAM

Figure 12. Package Mechanical Diagram



ORDERING INFORMATION

The order number for this part is:



Headquarters:

LinkUp Systems Corporation

1190 Coleman Av., Suite 2C
San Jose CA 95110
Tel: (408) 988-1848; Fax: (408) 988-3848
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3235 Kifer Road, Suite 110
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Tel: (408) 736-2260; Fax: (408) 736-2826
<http://www.ptsi.com>

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